REMARKS

The claims are claims 1, 4 to 7, 10, 11, 12 and 14 to 25.

Claims 22 to 26 erroneously numbered in the response filed September 12, 2006 have been re-numbered properly to claims 21 to 25.

Claims 1, 4 to 7, 10 to 12, 14 to 25 were rejected on the grounds of nonstatutory double patenting over claims 1 to 11 of U.S. Patent No. 6,738,888 by Chauvel, claims 1 to 13 of U.S. Patent No. 6,751,706 by Chauvel et al, claims 1 to 14 of U.S. Patent No. 6,889,330 by Chauvel et al, and claims 1 to 12 of U.S. Patent No. 6,901,521 by Chauvel et al. The Examiner states the subject matter claimed in this application is the same as the subject matter of a processing device for multitasking multiple tasks claimed in the patents and their claims pertain to the same subject matter as the pending claims in this application. Claims 1, 4 to 7, 10 to 12, 14 to 25 were also provisionally rejected on the grounds of nonstatutory double patenting over claims 1 to 15 of co-pending U.S. Patent Application No. 09/932,361. The Examiner states that disclosure and pending claims of the '361 application and this application claim the common subject matter of generating energy profiles for a specific task in a processing device executing multiple tasks and a processing device for multitasking multiple tasks.

Claims 1 and 7 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 1 and 7 recite "receiving hardware activity signals each indicative of a hardware event in the processing device." The '888 patent concerns modifying TLB entries and fails to make obvious receiving hardware activity signals. The '706 patent concerns a shared cache and fails to make obvious receiving hardware activity signals. The '330 patent concerns

configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious receiving hardware activity signals. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious receiving hardware activity signals. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious receiving hardware activity signals. Accordingly, claims 1 and 7 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 1 and 7 recite further subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claim 1 recites "counting hardware activity signals received during generation of said predetermined signal." Claim 7 similarly recites "each counter enabled to count said hardware activity signals when said comparator generates a corresponding predetermined second task identifier match signal." The '888 patent concerns modifying TLB entries and fails to make obvious this counting. The '706 patent concerns a shared cache and fails to make obvious this counting. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious this counting. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious this counting. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious this counting. Accordingly, claims 1 and 7 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 4 and 10 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the

'316 application. Claim 4 recites "periodically updating with a period T an energy profile responsive to said measuring step during operation of said processing device." Claim 10 recites the processing device operates "to periodically update with a period T an energy profile from counts of said plurality of counters during operation of said processing device." The '888 patent concerns modifying TLB entries and fails to make obvious this periodic update. The '706 patent concerns a shared cache and fails to make obvious this periodic update. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious this periodic update. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious this periodic update. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious this periodic update. Accordingly, claims 4 and 10 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 6 and 12 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claim 6 recites "performing a debugging operation responsive to said measuring step." Claim 12 recites the processing device includes "circuitry for implementing a debugging operation responsive to values in said plurality of counters." The '888 patent concerns modifying TLB entries and fails to make obvious this debugging operation. The '706 patent concerns a shared cache and fails to make obvious this debugging operation. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious this debugging operation. The '521 patent concerns enabling a circuit when any current task uses the circuit or

disabling the circuit when no task uses the circuit and fails to make obvious this debugging operation. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious this debugging operation. Accordingly, claims 6 and 12 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 14 and 20 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 14 and 20 recite the hardware events include "a cache miss." The '888 patent concerns modifying TLB entries and fails to make obvious that this hardware event is a cache miss. The '706 patent concerns a shared cache and fails to make obvious that this hardware event is a cache miss. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious that this hardware event is a cache miss. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious that this hardware event is a cache miss. The '361 application concerns modifying executing tasks reduce to heat generated by adjacent modules and fails to make obvious that this hardware event is a cache miss. Accordingly, claims 14 and 20 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 15 and 21 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 15 and 21 recite the hardware events include "a translation lookaside buffer miss." The '888 patent concerns modifying TLB entries and fails to make obvious that this hardware event is translation lookaside buffer miss. The '706 patent concerns a shared cache and fails to make obvious that this hardware event is a translation lookaside buffer miss. The '330

patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious that this hardware event is a translation lookaside buffer miss. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious that this hardware event is a translation lookaside buffer miss. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious that this hardware event is a translation lookaside buffer miss. Accordingly, claims 15 and 21 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 16 and 22 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 16 and 22 recite the hardware events include "a non-cacheable memory access." The '888 patent concerns modifying TLB entries and fails to make obvious that this hardware event is a non-cacheable memory access. The '706 patent concerns a shared cache and fails to make obvious that this hardware event is a non-cacheable memory access. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious that this hardware event is a non-cacheable memory access. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious that this hardware event is a non-cacheable memory access. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious that this hardware event is a non-cacheable memory access. Accordingly, claims 16 and 22 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 17 and 23 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 17 and 23 recite the hardware events include "a wait time." The '888 patent concerns modifying TLB entries and fails to make obvious that this hardware event is a wait time. The '706 patent concerns a shared cache and fails to make obvious that this hardware event is a wait time. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious that this hardware event is a wait time. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious that this hardware event is a wait time. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious that this hardware event is a wait time. Accordingly, claims 17 and 23 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 18 and 24 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 18 and 24 recite the hardware events include "a read/write request for a predetermined device." The '888 patent concerns modifying TLB entries and fails to make obvious that this hardware event is a read/write request for a predetermined device. The '706 patent concerns a shared cache and fails to make obvious that this hardware event is a read/write request for a predetermined device. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious that this hardware event is a read/write request for a predetermined device. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task

uses the circuit and fails to make obvious that this hardware event is a read/write request for a predetermined device. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious that this hardware event is a read/write request for a predetermined device. Accordingly, claims 18 and 24 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

Claims 19 and 25 recite subject matter not made obvious by the claims of the '888, the '706, the '330, the '521 patents or the '316 application. Claims 19 and 25 recite the period T "corresponds to a thermal time constant of the processing device." The '888 patent concerns modifying TLB entries and fails to make obvious that the period T is a thermal time constant of the processing device. The '706 patent concerns a shared cache and fails to make obvious that the period T is a thermal time constant of the processing device. The '330 patent concerns configuring circuits including a cache based upon stored attributes corresponding to the executing task and fails to make obvious that the period T is a thermal time constant of the processing device. The '521 patent concerns enabling a circuit when any current task uses the circuit or disabling the circuit when no task uses the circuit and fails to make obvious that the period T is a thermal time constant of the processing device. The '361 application concerns modifying executing tasks to reduce heat generated by adjacent modules and fails to make obvious that the period T is a thermal time constant of the processing device. Accordingly, claims 19 and 25 are allowable over the '888, '706, '330 and '521 patents and the '316 application.

The above lists particular limitations in particular claims that the Applicants believe are not shown in any reference patent or the reference application. The Applicants submit that in order to make a nonstatutory obviousness-type double patenting rejection

the Examiner must demonstrate how each limitation in the claims is made obvious by the claims of the reference patent or application. The Examiner has not made such a showing and provides only a vague statement that the claims of this application are similar to those of the reference patents and application. The FINAL REJECTION fails to state what portion of any reference makes obvious the limitations highlighted above. By this failure, the nonstatutory obviousness-type rejection is improper and should be withdrawn.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no Previously Presented search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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